<u> </u>			· ·			Sheet 1 o	
Form PTO- (Rev. 8-83)		epartment of Commerce at and Trademark Office	Atty Docket 0756		Serial No. 0	9/837,552	
I	NFORMATION DISCLOSURE ST	ATEMENT	Applicants: Hisashi Ol	HTANI et al.		seminario .	
			Filing Date: April 19, 2001		Group Art Unit:		
		U.S. PATENT	DOCUMENTS		Onusorgnou		
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate	
m 19 / 100	4,748,485	05/31/1988	Vasudev		1	(п арргоришто	
Mo	4,977,105	12/11/1990	Okamoto et al.				
201	4,984,033	01/08/1991	Ishizu et al.			•	
NOT W	4,996,575	02/26/1991	Ipri et al.				
PLY ST	4,996,575 5,034,788	07/23/1991	Kerr				
HON	5,103,277	04/07/1992	Caviglia et al.				
pa~	5,124,769	06/23/1992	Tanaka et al.				
400	5,140,391	08/18/1992	Hayashi et al.				
NON	5,185,535	02/09/1993	Farb et al.				
na	5,198,379	03/30/1993	Adan				
NOT	5,233,211	08/03/1993	Hayashi et al.				
NOR	5,246,882	09/21/1993	Hartmann				
Har	5,273,921	12/28/1993	Neudeck et al.				
200	5,275,972	01/04/1994	Ogawa et al.				
MUM	5,281,840	01/25/1994	Sarma				
MOR	5,294,821	03/15/1994	Iwamatsu				
pa	5,327,001	07/05/1994	Wakai et al.				
MU	5,359,219	10/25/1994	Hwang				
MR	5,371,398	12/06/1994	Nishihara				
204	5,420,048	05/30/1995	Kondo				
in	5,470,793	11/28/1995	Kalnitsky				
NON	5,475,238	12/12/1995	Hamada				
HON	5,506,436	04/09/1996	Hayashi et al.			 	
204	5,580,802	12/03/1996	Mayer et al.				
hor	5,604,368	02/18/1997	Taur et al.				
HOL	5,807,772	09/15/1998	Takemura				
NON	5,818,076	10/06/1998	Zhang et al.				
M	5,917,221	06/29/1999	Takemura				
700	6,054,734	04/25/2000	Aozasa et al.				

8/30/02

6,252,248

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

Yamazaki Sano et al.

09/02/1986

NON

SOU

Form	PTO-1449
(Rev.	8-83)



Atty Docket 0756-

Serial No. 09/837,552

INFORMATION DISCLOSURE STATEMENT

Applicants: Hisashi OHTANI et al.

Filing Date: April 19, 2001

Group Art Unit: **Unassigned**

FOREIGN PATENT DOCUMENTS

Examiner E	Document Number	Date	Country	Class	Subclass \	Translation Yes No
	0.470.447	04/23/1986	EP	1		Full Eng
	3 201 21 01-059866 01-059866	03/07/1989	JP			Eng Abst
NOT THE	02-015676	01/19/1990	JP			Eng Abst
NORTH	TRADE 02-666293	06/27/1997	JP			Full Eng
nan	03-082171	04/08/1991	JP			Eng Abst
MAN	03-256365	11/15/1991	JP			Eng Abst
\200~	04-152574	05/26/1992	JP			Eng Abst
120~	04-364074	12/16/1992	JP			Eng Abst
NOR	11-354802	12/24/1999	JP			Eng Abst
NDR	2000-183356	06/30/2000	JP			Full Eng
HUN	2000-194014	07/14/2000	JP			Full Eng
M	2000-196093	07/14/2000	JP			Full Eng
hor	57-032641	02/22/1982	JP			Eng Abst
NOR	58-115850	07/09/1983	JP			Full Eng
NA	60-081869	05/09/1985	JP			Eng Abst
HR	60-154660	08/14/1985	JP ·			Eng Abst
M	61-067269	04/07/1986	JP ·			Eng Abst
por	61-088565	05/06/1986	JP /			Eng Abst
PA)	61-220371	09/30/1986	JP			Eng Abst
pr /	62-005661	01/12/1987	JP			Eng Abst
MULY	62-117359	05/28/1987	JP			Full Eng
HON	64-019761	01/23/1989	JP			Eng Abst
HON	64-053459	03/01/1989	JP			Full Eng
200	64-053460	03/01/1989	JP			Full Eng
w	64-059866	03/07/1989	JP			Full Eng
FR	93/21659	10/28/1993	wo			Full Eng

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial Farrah et al., "Analysis of Double-Gate Thin-Film Transistor", pp. 69-74, February 1967, IEEE Transactions on Electron Devices, Vol ED-14, No. 2 Date Considered 🗸 Examiner

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

Applicants: Hisashi OHTANI et al. Filing Date: April 19, 2001 Group Art Unit: Unassigned OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Examiner Initial Ishii et al., "Experimental Fabrication of XMOS Transistors Using Lateral Solid-Phase Epitaxy of CVD Silicon Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Growth pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Materials, Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Le Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date: April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and Manufacturing Method Thereof", Filing Date: April 19, 2001, Shunpei YAMAZAKI et al.
Filing Date: April 19, 2001 Group Art Unit: Unaccigned OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Examiner Initial Ishii et al., "A Trial Product of Dual-Gate MOS (X MOS) Device", pp. 405, 1985, 46th Japan Society of Applied Physics, 2a-V-9 Ishii et al., "Experimental Fabrication of XMOS Transistors Using Lateral Solid-Phase Epitaxy of CVD Silicon Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Grown pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mater Tokyo, B-10-2 Hayashi, et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Journal of Applied Physics, Vol. 23, No. 11 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Le Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Data April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Examiner Initial Ishii et al., A Trial Product of Dual-Gate MOS (X MOS) Device", pp. 405, 1985, 46th Japan Society of Applied Physics, 2a-V-9 Ishii et al., "Experimental Fabrication of XMOS Transistors Using Lateral Solid-Phase Epitaxy of CVD Silicon Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Growth pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mater Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Jour of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Levol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Data April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Examiner Initial Ishii et al., A Trial Product of Dual-Gate MOS (X MOS) Device", pp. 405, 1985, 46th Japan Society of Applied Physics, 2a-V-9 Ishii et al., "Experimental Fabrication of XMOS Transistors Using Lateral Solid-Phase Epitaxy of CVD Silicon Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Grown pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mater Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Jour of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extend Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Le Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Ishii et al., "A Trial Product of Dual-Gate MOS (X MOS) Device", pp. 405, 1985, 46th Japan Society of Applied Physics, 2a-V-9 Ishii et al., "Experimental Fabrication of XMOS Transistors Using Lateral Solid-Phase Epitaxy of CVD Silicon Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Growth pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mater Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Jour of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Levol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Data April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Films", pp. L521-L523, April 1990, Japanese Journal of Applied Physics, Vol. 29, No. 4 Noguchi et al., "Advanced High Mobility Polysilicon Super-thin Film Transistor (SFT) Using Solid Phase Growt pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mate Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Jou of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Levol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Data April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
pp. 549-552, 1986, Extended Abstracts of the 18th International Conference on Solid State Devices and Mate Tokyo, B-10-2 Hayashi et al., "Polysilicon Super-Thin-Film Transistor (SFT)", pp. L819-L820, November 1984, Japanese Jou of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extendadostracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Le Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Data April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
of Applied Physics, Vol. 23, No. 11 Hayashi et al., "High Performance Superthin Film Transistor (SFT) with Twin Gates", pp. 59-62, 1987, Extended Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Level Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Abstracts of the 19th Conference on Solid State Devices and Materials, Tokyo, A-3-5 Sekigawa et al., "The Development of XMOS Transistor", pp. 44-49, 1986, Semiconductor World Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Levol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Tuan et al., "Dual-Gate a-Si:H Thin Film Transistors", pp. 357-359, December 1982, IEEE Electron Device Le Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Vol. EDL-3, No. 12 Specifications and Drawings for Patent Application Serial No. 09/837,877, "Semiconductor Device", Filing Date April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
April 19, 2001, Shunpei YAMAZAKI et al. Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and
Specifications and Drawings for Patent Application Serial No. 09/837,558, "Semiconductor Device and Manufacturing Method Thereof", Filing Date: April 19, 2001, Shunpei YAMAZAKI et al.
· ·
Examiner of 29-101/03 Date Considered 10/1/03
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this formwith next communication to applicant.

08/13/2001

PTO/SB/08A (08-00) Approved for use through 10/31/2002. OMB 0651-0031

Under the Paperwork Reduction Act of 1995, no persons are required to a collection of information unless it contains a valid OMB control number.

Substitute	for form 1449A/PTO			Com	iplete i	if Known
INFO	RMATION I	DISC	LOSURE	Application Number		09/837,552
STATEMENT BY APPLICANT			Filing Date		April 19, 2001	
		First Named Inventor		Aisashi OHTANI et al.		
(use as many sheets as necessary)			Group Art Unit	- (Unassigned	
	Examiner Name		Examiner Name		Unassigned	
Sheet	1	of	1	Attorney Docket Number		0756-2296

			U.S. PATENT DOCUMENT	S		
Examiner Initials	Cite No. 1	U.S. Patent Document	Name of Patentee or Applicant of Cited	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevan Passages or Relevant Figures Appear	
		Number Kind Code ² (if known,	Document			
por		4,609,930	Tsuneo YAMAZAKI et al.	09/02/1986		
	/					
/ .						

				FC	REIGN PATENT DOC	UMENTS		
Examiner Initials*	Cite No.1	Fo Office ³	reign Patent Doc Number ⁴	ument Kind Code ³ (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T⁵
	+	 						
	 							
					· / -			
			'					
			отн	ER PRIOR A	ART – NON PATENT LITE	RATURE DOCUMENTS		•
Examiner Initials	Cite No.1				or (in CAPITAL LETTERS), t irnal, serial, symposium, catalo publisher, city and/or count	og, etc.)., date, page(s), volum		T ²
							·	╄—
								1
				,	·			
				11				
			7×7	/ //				
Examiner	111	A)-	1 16	//	Da	ite //		

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Considered

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

Signature

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

¹Unique citation designation number. ²Applicant is to place a check mark here if English language Translation is attached.